IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, and wherein the low tunnel barrier intergate insulator is separated from the control gate by a first metal layer.

2. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

3. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

4. (Original) The floating gate transistor of claim 3, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a Perovskite oxide tunnel barrier.

6. (Currently Amended) The floating gate transistor of claim 1, wherein the floating gate includes a polysilicon floating gate having a second metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

7. (Currently Amended) The floating gate transistor of claim 6, wherein the control gate includes a polysilicon control gate having the first ~~a~~ metal layer formed thereon in direct contact with the low tunnel barrier intergate insulator.

8. (Original) The floating gate transistor of claim 1, wherein the floating gate transistor includes an n-channel type floating gate transistor.

9. (Currently Amended) A vertical non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, the low tunnel barrier intergate insulator being separated from the control gate by a first metal layer.

10. (Previously Presented) The vertical non volatile memory cell of claim 9, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

11. (Currently Amended) The vertical non volatile memory cell of claim 9, wherein the floating gate includes a polysilicon floating gate having a second metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

12. (Currently Amended) The vertical non volatile memory cell of claim 11, wherein the control gate includes a polysilicon control gate having the first ~~a~~ metal layer formed thereon in direct contact with the low tunnel barrier intergate insulator.

13. (Previously Presented) The vertical non volatile memory cell of claim 9, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

14. (Previously Presented) The vertical non volatile memory cell of claim 13, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

15. (Previously Presented) The vertical non volatile memory cell of claim 9, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

16. (Previously Presented) The vertical non volatile memory cell of claim 15, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

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17. (Currently Amended) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the first metal layer;

a second metal layer formed on the metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.

18. (Previously Presented) The non-volatile memory cell of claim 17, wherein first and the second metal layers are lead and the metal oxide intergate insulator is lead oxide (PbO).

19. (Currently Amended) The non-volatile memory cell of claim 17, wherein the first and second metal ~~layer~~ layers are aluminum and the metal oxide intergate insulator is aluminum oxide (Al_2O_3).

20. (Previously Presented) The non-volatile memory cell of claim 17, wherein the first and the second metal layers include transition metal layers and the metal oxide intergate insulator includes a transition metal oxide intergate insulator.

21. (Previously Presented) The non-volatile memory cell of claim 20, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

22. (Previously Presented) The non-volatile memory cell of claim 20, wherein the metal oxide intergate insulator includes a Perovskite oxide intergate insulator.

23. (Previously Presented) The non-volatile memory cell of claim 17, wherein the floating gate transistor includes a vertical floating gate transistor.

24. - 80. (Canceled)

81. (New) The floating gate transistor of claim 1, wherein the low tunnel barrier integrate insulator includes a metal oxide insulator consisting of lead oxide (PbO).

82. (New) The floating gate transistor of claim 3, wherein the transition metal oxide is Ta_2O_5.

83. (New) The floating gate transistor of claim 3, wherein the transition metal oxide is TiO_2.

84. (New) The floating gate transistor of claim 3, wherein the transition metal oxide is Nb_2O_5.

85. (New) The floating gate transistor of claim 7, wherein the insulator is a metal oxide insulator layer and the metal layers include the same metal material used to form the metal oxide insulator layer.

86. (New) The vertical non volatile memory cell of claim 12, wherein the insulator is a metal oxide insulator layer and the metal layers include the same metal material used to form the metal oxide insulator layer.

87. (New) The non-volatile memory cell of claim 17, wherein the first and second metal layers include the same metal material used to form the metal oxide insulator layer.

88. (New) A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, the low tunnel barrier intergate insulator including a Perovskite oxide tunnel barrier.

89. (New) A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, the control gate including a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

90. (New) A vertical non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator, the control gate including a polysilicon control gate having a first metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

91. (New) The vertical non volatile memory cell of claim 90, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator comprising PbO.

92. (New) The vertical non volatile memory cell of claim 90, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator comprising Ta_2O_5.

93. (New) The vertical non volatile memory cell of claim 90, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator comprising TiO_2.

94. (New) The vertical non volatile memory cell of claim 90, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator comprising Nb_2O_5.

95. (New) A vertical non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide, the floating gate including a horizontally oriented floating gate formed alongside of the body region;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

96. (New) The vertical non volatile memory cell of claim 95, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

40 97. (New) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the first metal layer;

a second metal layer formed on the metal oxide intergate insulator, wherein the first and the second metal layers are lead and the metal oxide intergate insulator is lead oxide (PbO); and

a polysilicon control gate formed on the second metal layer.

41 98. (New) A non-volatile memory cell, comprising:

B1 a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the first metal layer;

a second metal layer formed on the metal oxide intergate insulator, the first and the second metal layers include transition metal layers and the metal oxide intergate insulator includes a transition metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.

42 99. (New) The non-volatile memory cell of claim 41, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

43 100. (New) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

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a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the first metal layer, the metal oxide intergate insulator includes a Perovskite oxide intergate insulator;

a second metal layer formed on the metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.